

**A Better Hybrid Bonding Process**: Rapid advancements in AI and high-performance computing (HPC) have made high bandwidth memory (HBM) and more efficient logic/memory device interconnections critical. Traditional packaging approaches use solder bump technology to form interconnections between dies and memory components. But as the input/output (I/O) count increases and fine-pitch requirements become more urgent, the reliability and yield challenges associated with solder bump technology have increased. That’s why hybrid bonding, which enables the simultaneous bonding of dielectric and metal pads, has emerged as a promising solution. It can accommodate fine-pitch interconnections with superior reliability. However, issues with commonly used oxide-based hybrid bonding approaches pose a significant barrier to its adoption in mass production. The main issues are the high cost of the multiple steps of the CMP process used, and the low tolerance of surface topography.

At ECTC, a National Yang Ming Chiao Tung Univ.-led team will describe a different hybrid bonding approach – Cu/polymer hybrid bonding. They say it offers both lower cost and a broader process window, and achieves results similar to oxide-based approaches. They demonstrated a 30-second, 150-200°C Cu/polymer hybrid bonding process with a) a low-cost, wide process window (surface roughness 2~20 nm) and b) high-throughput (< 30-second bonding duration) for high I/O applications.

* **The image above** is a cross-sectional SEM analysis of Cu/polymer hybrid bonding under 180°C for 30 seconds.

**(Paper 32.3, “*Ultra-Fast Cu/Polymer Hybrid Bonding with Electroless Passivation Layer for Cost-Effective High I/O Interconnection Stacking,”* Yu-Lun Liu et al, National Yang Ming Chiao Tung Univ./ Tokyo Ohka Kogyo Co. LTD)**